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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/464,811	12/17/99	SHAO	H 1-10-3

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DOCKET ADMINISTRATOR (RM 3C-512)
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EXAMINER	
CRUZ,L	
ART UNIT	**PAPER NUMBER**
2815	5

DATE MAILED: 01/03/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)

1- File Copy

*U.S. GPO: 2000-473-000/44602

Office Action Summary	Application No.	Applicant(s)	
	09/464,811	SHAO ET AL.	
	Examiner	Art Unit	
	Lourdes C. Cruz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *20 October 2000* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *22-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

This Office Action is in response to an Amendment filed October 20,2000.

Applicant's election with traverse of claims 1-21 in Paper No. 2 is acknowledged. The traversal is on the ground that selectively depositing the layer so that etching is not necessary does not suggest another method for producing the same claimed semiconductor device. This is not found persuasive because the above does in fact propose another method for producing the semiconductor device as claimed.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeng et al. (U.S. Patent No. 5818111).

Regarding claim 1, Jeng et al. disclose:

a semiconductor structure comprising a first upper level of interconnect members formed (See Fig. 3) over a semiconductor layer (10) having an electronic device formed thereon; at least one lower level of interconnect members formed between the semiconductor layer and the first upper level (See col. 4, lines 43+);

a first insulative material (18), having a relatively low dielectric constant (Col. 5, Table), positioned to electrically isolate members of the first upper level from one another and extending to the lower level of interconnect members; and

a second insulative material (22) having a relatively high dielectric constant (See Col. 5, Table), positioned to electrically isolate members of the lower level from the electronic device (Col. 3, lines 53+).

With regard to claim 2, Jeng et al. disclose the semiconductor structure of claim 1 wherein a portion of the second insulative material (22) extends between an interconnect member of the lower level and an interconnect member of the upper level.

Regarding claim 3, Jeng et al. disclose the structure of claim 1 wherein the second insulative material (22) predominantly comprises silicon dioxide (Col. 5, Table) and the structure further includesa plurality of individual portions formed of the second insulative material, each portion extending between a member of the lower level and a member of the upper level and self-aligned with said member of the upper level.

Regarding claim 4, Jeng et al. disclose the structure of claim 1 including at least a second upper level of interconnect members formed over the first upper level (Col. 4, lines 43+).

Regarding claim 6, Jeng et al. disclose the structure of claim 1 wherein members of the first level (14) comprise Al,the first insulative material (18) comprises hydrogen silsesquioxane (Col. 5, Table) and the second insulative material (22) comprises silicon dioxide (Col. 5, Table).

Regarding claim 7, Jeng et al. disclose the structure of claim 1 further including a second upper level of interconnect members formed between the first upper level of interconnect members and the lower level of interconnect members (Col. 4, lines 43+) wherein potions of the lower insulative material electrically isolate the second upper level of interconnect members from the lower level of interconnect members.

Regarding claim 8, Jeng. et al. disclose the structure of claim 1 further including:

a plurality of additional upper levels of interconnect members formed between the first upper level and the lower level (Col. 4, lines 43+);

a first layer formed of the first insulative material (18) and positioned between the first upper level and a first of the additional levels (Col.4, lines 43+); and

a second layer formed of the first insulative material and positioned between second and third ones of the additional levels.

Regarding claim 9, Jeng et al. disclose the structure of claim 1 comprising second third, fourth and fifth upper levels of interconnect members formed between the first upper level and the lower level (Col. 4, lines 43+)

Regarding claim 10, Jeng et al. disclose the structure of claim 9 wherein the first, second, third, fourth and fifth upper levels are electrically isolated from one another by a continuous layer comprising the first insulative material (18).

Regarding claim 11, Jeng et al. disclose the structure of claim 9 wherein the first insulative material (18) is a single species of low k dielectric material (Col. 5, Table) and the second insulative material (22) predominantly comprises silicon dioxide (Col. 5, Table).

Regarding claim 12, Jeng et al. disclose the structure of claim 9 wherein multiple layers each comprising the first insulative material (18) electrically isolate the first, second, third, fourth and fifth upper levels from one another (Col. 4, lines 43+).

Regarding claim 13, Jeng et al. discloses the structure of claim 1 further including a second upper level of interconnect members formed between the first level of interconnect members and the lower level of interconnect members (14) wherein portions of the second insulative material (22) extend to electrically isolate the second upper level of interconnect members from the lower level of interconnect members (See Fig. 3).

With regard to claim 14, Jeng et al disclose the structure of claim 12 wherein portions of the second insulative material (22) extend between two or more of the upper levels.

With regard to claim 15, Jeng et al. disclose the structure of claim 1 further including:

a first plurality of conductive portions (16) extending at least between the upper level of interconnect and the lower level of interconnect; and a second plurality of conductive portions (16) extending at least between the lower level of interconnect and some of the electronic devices (Col. 3, lines 53+)

With regard to claim 16, Jen et al. disclose the structure of claim 15 wherein the first plurality of conductive potrtions are integrally formed with members of the first upper level in (See Fig. 3) a dual Damascene structure in so much as "dual Damascene" structure denotes any specific structure or structural limitation.

Regarding claim 17, Jen et al. disclose the structure of claim 15 wherein all of the members (14) predominately comprise Al (See Fig. 3).

Regarding claim 18, Jeng et al. disclose the structure of claim 1 wherein the first insulative material extends from the first upper level to electrically isolate members of the lower level from one another (See Fig. 3).

Regarding claim 19, jeng et al. disclose the structure of claim 1 further including at least a second upper level of interconnect members (Col. 4, lines 43+) formed over the first upper level of interconnect members with the first insulative material (18) extending from the first upper level to electricallly isolate members (14) of the second upper level from one another.

With regard to claim 20, Jeng et al. disclose a semiconductor structure comprising:

A first upper level of interconnect members formed over a semiconductor layer (10); a lower level of interconnect members (14) formed between the semiconductor layer and the first upper level (Col. 4, lines 43+); and insulative (18) positiones to electrically isolate portions of the upper level of interconnect members (14) from one another, portions of the upper level of interconnect members (14) from portions of the lower level of interconnect members and portions of the lower level of interconnect members (14) from one another,

Said insulative material (18) comprising a continuous layer extending from within regions between members of the upper level of interconnect to within regions between

members of the lower level of interconnect (See Fig. 3) said continuous layer characterized by a dielectric constant of less than 3.9 (Col. 5, Table).

Also regarding claims 1,5, and 20, see In re Pearson 181 USPQ 641 (CCPA) which makes clear that terms merely setting forth intended use for, or a property inherent in, an otherwise old composition do not differentiate claimed composition from those known to prior art. See also, In re Swinehart [169 USPQ 226] (CCPA 1971) which makes clear that mere recitation of a newly discovered function or property, inherently possessed by things in prior art, does not cause claim drawn to those things to distinguish over prior art.

Response to Arguments

Applicant's arguments filed October 27, 2000 have been fully considered but they are not persuasive. Applicant's arguments regarding restriction requirement have been considered and are found not persuasive. They are addressed above under the Election/Restriction heading.

Regarding the Rejections under Section 102, the rejection is proper and Jeng does anticipate the disclosed inventioned as claimed. Applican't claims are not found to be patentable over '111 because Jeng teaches the features claimed by the Applicant as discussed above. Layer 18 satisfies the structural requirements of Applicant's claims and '111's SiO layer reads on the claims as drafted by Applicant.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jeng (U.S. Patent No. 6054769) discloses a low capacitance interconnect structure. Jeng (U.S. Patent No. 5858871) discloses a porous insulator for capacitance reduction. Chen et al. (U.S. Patent No. 5976984) disclose a process of making unlanded vias. Jeng (U.S. Patent No. 5548159) discloses a line to line capacitance reduction insulator. Dawson et al. (U.S. Patent No. 5783864) disclose a multtilayer interconnect structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lourdes C. Cruz whose telephone number is 707-306-5691. The examiner can normally be reached on M-F 8:00- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Lourdes C. Cruz
Examiner
Art Unit 2815

Lourdes Cruz
December 29, 2000

Jerome Jackson, Jr.
Primary Examiner